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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/313,424	05/17/1999	THOMAS HUTTNER	GR-98-P-8041	3890

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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/313,424	HUTTNER ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 16-25* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-21 and 23-25* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The rejection that set was forth in Paper No. 28 is maintained and repeated herein below as record.

Claim 18 recited the limitation "wherein the introducing step is performed such tha there is an implantation maximum for the passivating substance X in the vicinity of the interface. However, it is not clear to the Examiner how is **the implantation maximum is defined** for the **passivating substance in the vicinity of the interface**. Is that the maximum concentration ? Is that the maximum depth of implantation? And so forth. As result the claim lacks clarity in its scope and meaning. Therefore, the claim is indefinite in its scope and meaning.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16- 21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over unpatentable Hsu (US/5,468,657) in view of Sato et al. (USPAT/6,121,117).

The rejection that set was forth in Paper No. 28 is maintained and repeated herein below as record.

Re claim 16 -19 Hsu teaches a method of fabricating a semiconductor configuration comprising: providing a semiconductor structure (see Fig. 4) having a base layer (44), an insulation layer (59), and a monocrystalline silicon layer (3); introducing a passivating substance X (not labeled) (i.e., ion-implanting) between the insulation layer (59) and the monocrystalline silicon layer (3) having maximum implant concentration of X substance; and heat-treating the semiconductor structure with the passivating substance X, thereby, causing the passivating substrate diffuse into an interface between the insulation layer (59) and the monocrystalline silicon layer (3) (see Fig. 4 and Col. 7, lines 24-45).

However, Hsu does not specifically disclose limitations of providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from a group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer.

Sato et al. disclose providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer in order to form SOI (see Figs. 2A-2D).

Sato et al. suggest that "formation of mono-crystalline Si semiconductor layer on an insulator is well known as silicon-on-insulator (SOI) technique. Many investigations have been made thereon since the devices made by the SOI technique have many advantages which are not achievable with a bulk Si substrate for usual Si integrated circuits. The advantages brought about by the SOI technique are as below: 1. Ease of dielectric separation, and practicability of high integration, 2. High resistance against radioactive rays, 3. Low floating capacity, and practicability of high speed operation, 4. Practicability of omission of a welling step, 5. Practicability of prevention of latching-up, 6. Practicability of thin film formation for complete depletion type field effect transistor, and so forth." (see Sato et al. Col. 3, lines 42-59) One of ordinary skill in the art would have motivated to use SOI technique as Sato et al. disclosed in order to improve the overall device performance and applicability of the device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Hsu reference with SOI technique as taught by Sato et al. because the device performance would have been improved.

Re claim 20, as applied to claim 16 above, Hsu and Sato et al. in combination teach all the claimed limitations including the limitation of forming a covering oxide layer (68) on the monocrystalline silicon layer (see Fig. 5).

Re claim 21, as applied to claim 16 above, both Hsu and Sato et al. in combination teach all the claimed limitations including the limitation of patterning the monocrystalline silicon layer by etching away regions thereof down to the underlying insulation layer (see Hsu Figs. 4 and 5).

Re claim 23, as applied to claim 21 above, both Hsu and Sato et al. in combination teach all the claimed limitations including wherein the patterning step performed before the step of introducing the passivating substance X into one of an insulation layer and the monocrystalline silicon layer (see Hsu Figs. 4 and 5).

Re claim 24, as applied to claim 16 above, Hsu and Sato et al. in combination teach all the claimed limitations including the limitation of doping the monocrystalline silicon layer differently region by region by means of ion implantation; and performing the doping step after the step of introducing the passivating substance X and the heat-treating step (see Col. 8, lines 17-67).

Re claim 25, as applied to claim 21 above, both Hsu and Sato et al. in combination teach all the claimed limitations including wherein the step of introducing the passivating substance X into monocrystalline silicon layer is performed such that an implanted does of the passivating substance X is below an amorphizing dose of silicon (see Hsu Figs. 4 and 5).

Allowable Subject Matter

5. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 21, 23 and 25 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicants' arguments filed on May 5, 2003, with respect to claims 16-20 and 24, have been fully considered but they are not persuasive.

Applicants response with respect to rejection of claim 18 under 35 U.S.C. § 112 second Paragraph is still not persuasive. As applied in Paragraph 2 here in above, the Examiner still have had difficulty to understand what is actually being claimed. Although the claimed limitation has support in the specification, as correctly pointed out by the applicants, the specification does not provide any meaning or explanation how the claimed limitation can be interpreted by one of ordinary skill in the art. Therefore, the rejection under 35 U.S.C. § 112 second Paragraph is still deemed proper.

Regarding rejection of claims 16-21 and 23-25 under 35 U.S.C. § 103, applicants argued that "Fig. 4 Hsu shows, a wafer 20 and upper layer 42 monocrystalline silicon, a middle layer 59 of nitrogen-implanted silicon dioxide, and lower monocrystalline silicon ... *Hsu* the nitrogen is implanted into the silicon dioxide layer which is an insulator... there is no disclosure of suggestion in either *Hsu et al.* of *Sato et al.* introduce passivating substance into a monocrystalline silicon layer..."

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. As stated above, in part, applicants' argument is very confusing. In one hand applicants are admittedly showing that layer 42 in Hsu et al. reference is monocrystalline silicon layer, in other hand applicants are arguing Hsu et al. do not teach "passivating substance" (i.e., nitrogen ion implant) into the monocrystalline. As shown Fig. 4, as applicants correctly pointed out, Hsu et al. discloses an SOI substrate comprises the first layer (44) of monocrystalline silicon the second layer (59) of silicon oxide formed directly on the first layer and the third layer (42) of monocrystalline silicon. As figure 4 shows, the third layer (20) of the monocrystalline silicon layer is implanted with a nitrogen ion ("passivating substance") and the nitrogen penetrates through the third layer of monocrystalline silicon (20) and goes deep into the second layer of silicon oxide (59) (i.e., monocrystalline silicon also implanted). Therefore, Examiner respectfully submits that Hsu et al. disclose introducing of "passivating substance", i.e., nitrogen ion, into a monocrystalline silicon layer. And applicants' argument has no merit given clear discloser of Fig. 4. See also *Semiconductor Energy Laboratory Co. V. Samson Electronics Co.* 54 USPQ2d 1001 (CA FC 2000). Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Further, in response to applicants' arguments against the references individually, one cannot show non-obviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In addition, Applicants' arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

Finally, applicants' arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
July 5, 2003

W. David Coleman
Primary Examiner